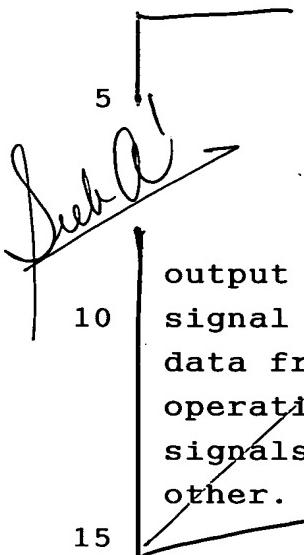


WHAT IS CLAIMED IS:



1. An electronic instrument comprising:  
a memory device; and  
strobe signal lines through which a first  
output strobe signal and a second output strobe  
signal are transmitted in synchronism with output  
data from said memory device in the data output  
operation, the first and second output strobe  
signals being in complementary relation to each  
other.
2. The electronic instrument as claimed  
in claim 1, wherein said memory device has a strobe  
output buffer that generates the first and second  
output strobe signals based on a predetermined  
signal, the first and second output strobe signals  
being supplied from said strobe output buffer to  
said strobe signal lines when the output data is  
output from said memory device.

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3. The electronic instrument as claimed  
in claim 1, wherein the first and second output  
strobe signals have different levels in a preamble  
time which is a time period before a head of a cross  
point train of the first and second output strobe  
signals, the head of the cross point corresponding  
to a start of a strobe period of the first and

24

second output strobe signals.

5

4. The electronic instrument as claimed  
in claim 3, wherein the first and second output  
strobe signals have different levels in a 'postamble'  
time which is a time period after a cross point of  
10 the first and second output strobe signals which  
cross point corresponds to an end of a strobe period  
of the first and second output strobe signals.

15

5. The electronic instrument as claimed  
in claim 3, wherein the levels of the first and  
second output strobe signals in the preamble time  
20 are set by use of a read command as a trigger.

25

6. The electronic instrument as claimed  
in claim 3, wherein the levels of the first and  
second output strobe signals in the preamble time  
are set a predetermined time before a first output  
data item is output.

30

7. The electronic instrument as claimed  
35 in claim 6, wherein transistors of said memory  
device which transistors drive the strobe signal  
lines are controlled to be in a off state in a

25

waiting time period.

5

8. The electronic instrument as claimed  
in claim 1, wherein each of cross points of the  
first and second output strobe signals is set at an  
edge trigger point of a corresponding one of output  
10 data items.

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9. The electronic instrument as claimed  
in claim 1, wherein each of cross points of the  
first and second output strobe signals is set at a  
center point of a corresponding one of output data  
items.

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10. An electronic instrument comprising:  
a memory device; and  
strobe signal lines through which a first  
input strobe signal and a second input strobe signal  
are transmitted in synchronism with input data  
supplied to said memory device in the data input  
operation, the first and second input strobe signals  
being in complementary relation to each other.

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8 11. The electronic instrument as claimed  
in claim 10, wherein said memory device has a strobe

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input buffer that receives the first and second  
input strobe signals transmitted through said strobe  
signal lines and generates, based on the first and  
second input strobe signals, a strobe clock signal  
5 used to settle input data items supplied to said  
memory device.

10

~~10~~ 12. The electronic instrument as claimed  
in claim ~~10~~, wherein the first and second input  
strobe signals have different levels in a preamble  
time which is a time period before a head of a cross  
15 point train of the first and second input strobe  
signals, the head of the cross point corresponding  
to a start of a strobe period of the first and  
second input strobe signals.

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~~10~~ 11 13. The electronic instrument as claimed  
in claim ~~12~~, wherein the first and second input  
strobe signals have different levels in a postamble  
time which is a time period after a cross point of  
the first and second input strobe signals which  
cross point corresponds to an end of a strobe period  
of the first and second input strobe signals.

30

~~10~~ 12 14. The electronic instrument as claimed  
35 in claim ~~12~~, wherein the levels of the first and  
second input strobe signals in the preamble time are  
set by use of a write command as a trigger.

13  
15. The electronic instrument as claimed  
in claim 10, wherein the levels of the first and  
second input strobe signals in the preamble time are  
set a predetermined time before a first input data  
5 item is received.

10 14  
16. The electronic instrument as claimed  
in claim 15, wherein transistors of a unit supplying  
the input data to said memory device which  
transistors drive the strobe signal lines are  
controlled to be in a off state in a waiting time  
15 period.

20  
17. The electronic instrument as claimed  
in claim 10, wherein each of cross points of the  
first and second input strobe signals is set at an  
edge trigger point of a corresponding one of input  
data items.

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18. The electronic instrument as claimed  
in claim 10, wherein each of cross points of the  
first and second input strobe signals is set at a  
center point of a corresponding one of input data  
items.

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*Sub A 3*

19. An electronic instrument comprising:  
a memory device; and  
strobe signal lines through which a first  
output strobe signal and a second output strobe  
signal are transmitted in synchronism with output  
data from said memory device in a data output  
operation and a first input strobe signal and a  
second input strobe signal are transmitted in  
synchronism with input data supplied to said memory  
device in a data input operation, the first and  
second output strobe signals being in complementary  
relation to each other, the first and second input  
strobe signals being in complementary relation to  
each other.

15

*16*  
20. The electronic instrument as claimed  
in claim 19, said memory device comprises:

a strobe output buffer that generates the  
first and second output strobe signals based on a  
predetermined signal, the first and second output  
strobe signals being supplied from said strobe  
output buffer to said strobe signal lines when the  
output data is output from said memory device; and  
a strobe input buffer that receives the  
first and second input strobe signals transmitted  
through said strobe signal lines and generates,  
based on the first and second input strobe signals,  
a strobe clock signal used to settle input data  
items supplied to said memory device.

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*17*

21. The electronic instrument as claimed

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in claim 19, wherein the first and second output strobe signals have different levels in a first preamble time which is a time period before a head of a cross point train of the first and second  
5 output strobe signals, the head of the cross point corresponding to a start of a strobe period of the first and second output strobe signals, and wherein the first and second input strobe signals have different levels in a second preamble time which is  
10 a time period before a head of a cross point train of the first and second input strobe signals, the head of the cross point corresponding to a start of a strobe period of the first and second input strobe signals.

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17 22.

20 The electronic instrument as claimed in claim 21, wherein the first and second output strobe signals have different levels in a first postamble time which is a time period after a cross point of the first and second output strobe signals which cross point corresponds to an end of a strobe  
25 period of the first and second output strobe signals, and wherein the first and second input strobe signals have different levels in a second postamble time which is a time period after a cross point of the first and second input strobe signals which  
30 cross point corresponds to an end of a strobe period of the first and second input strobe signals.

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18 23. The electronic instrument as claimed in claim 22, wherein said strobe signal lines

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includes output strobe signal lines through which the first and second output strobe signals and input strobe signal lines through which the first and second input strobe signal lines, said output strobe  
5 signal lines and said input strobe signal lines being separated from each other, wherein when an even number of consecutive output data items are output, the levels of the first and second output strobe signals are controlled in a waiting time  
10 period to be maintained at the same levels as in the first postamble time, and wherein when an even number of consecutive input data items are supplied, the levels of the first and second input strobe signals are controlled in a waiting time period to  
15 be maintained at the same levels as in the second postamble time.

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*20*  
*24.* The electronic instrument as claimed in claim *22*, wherein said strobe signal lines includes output strobe signal lines through which the first and second output strobe signals and input  
25 strobe signal lines through which the first and second input strobe signal lines, said output strobe signal lines and said input strobe signal lines being separated from each other, wherein when an odd number of consecutive data output items are output,  
30 the levels of the first and second output strobe signals are controlled in a waiting time period to be maintained at the same levels as in the first postamble time and then restored at the start of the second preamble time in the next data read operation.

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25. A semiconductor memory device provided in an electronic instrument having clock lines through which complementary clock signals are transmitted to be used for synchronization of a data output operation for said semiconductor memory device, and strobe signal lines through which a first output strobe signal and a second output strobe signal are transmitted to be used to settle output data from said semiconductor memory device in 10 the data output operation, the first and second output strobe signals being in complementary relation to each other, said semiconductor memory device comprising:

15 a data output buffer that outputs the output data from a memory bank; and  
a strobe output buffer that generates the first and second output strobe signals based on a predetermined signal, the first and second output strobe signals being supplied from said strobe 20 output buffer to said strobe signal lines when the output data is output from said data output buffer.

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26. A semiconductor memory device provided in an electronic instrument having clock lines through which complementary clock signals are transmitted to be used for synchronization of a data input operation for said semiconductor memory device, and strobe signal lines through which a first input strobe signal and a second input strobe signal are transmitted to be used to settle input data supplied to said semiconductor memory device in the data 30 input operation, the first and second input strobe signals being in complementary relation to each other, said semiconductor memory device comprising:  
35

a strobe input buffer that receives the first and second input strobe signals transmitted through said strobe signal lines and generates a strobe clock signal based on the first and second input strobe signals; and

a data input buffer that receives input data items supplied to said semiconductor memory device, the input data items being settled by using the clock strobe signal generated by said input strobe buffer.

## 10 strobe buffer.

15           27. A semiconductor memory device  
provided in an electronic instrument having clock  
lines through which complementary clock signals are  
transmitted to be used for synchronization of a data  
output operation and a data input operation for said  
20 semiconductor memory device, and strobe signal lines  
through which a first output strobe signal, a second  
output strobe signal, a first input strobe signal  
and a second input strobe signal are transmitted to  
be used to settle output data from said memory  
25 device in the data output operation and to settle  
input data supplied to said semiconductor memory  
device, the first and second output strobe signals  
being in complementary relation to each other, the  
first and second input strobe signals being in  
30 complementary relation to each other, said memory  
device comprising:

a data output buffer that outputs the output data from a memory bank;

35 a strobe output buffer that generates the  
first and second output strobe signals based on a  
predetermined signal, the first and second output  
strobe signals being supplied from said strobe

output buffer to said strobe signal lines when the output data is output from said data output buffer;

5           a strobe input buffer that receives the first and second input strobe signals transmitted through said strobe signal lines and generates a strobe clock signal based on the first and second input strobe signals; and

10          a data input buffer that receives input data items supplied to said semiconductor memory device, the input data items being settled by using the clock strobe signal generated by said input strobe buffer.

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